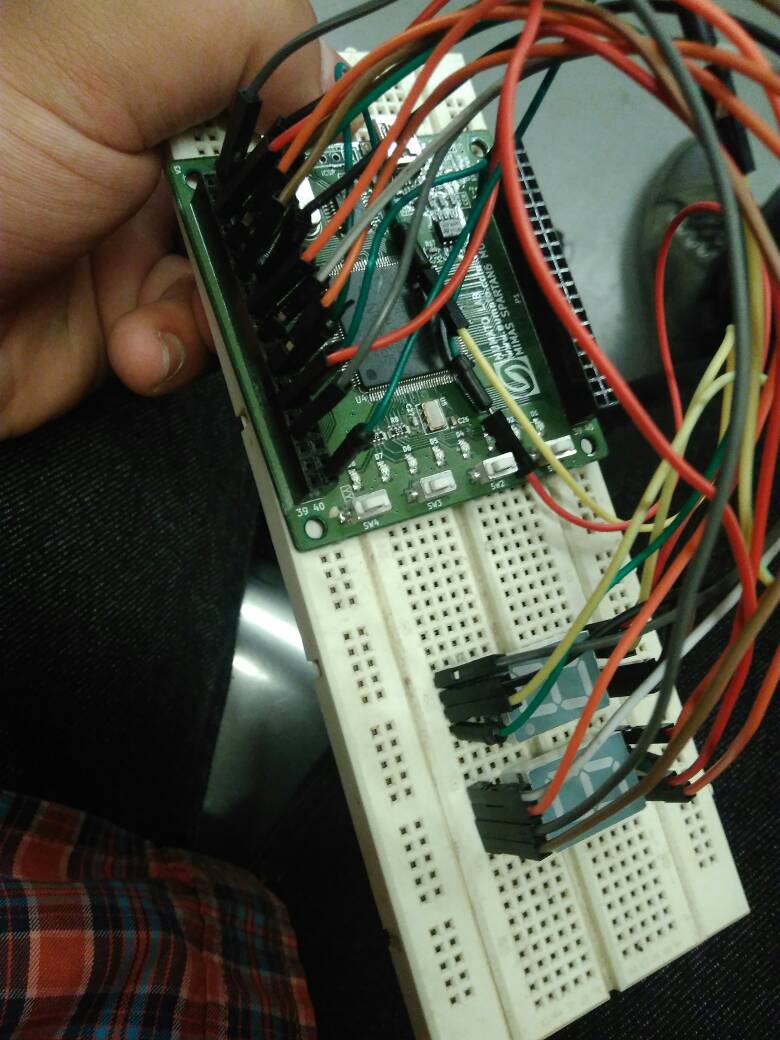
EMBEDDED SYSTEMS STUDIO-II

LAB PROJECT



IMPLEMENTATION OF REACTION TIMER ON SPARTAN 6 FPGA

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**Introduction**

Embedded Systems Studio VI.5.2 paper deals with topics VHDL language, Concurrent and Sequential Assignment, Embedded Hardware specification, FPGA Architecture and others. Thus indulging us in practical that include embedded hardware and rigorous hardware description language.

Following practicals were taken up:

1. *Reaction Timer*: An electronic setup for calculating quick reaction time with help of counter.

2. *Dice Game*: An electronic dice game, wherein you have 2 die to roll.

3. *Microprocessor*: A simulation of a CPU, comprising of registers, buffer memory for operations to be held on operands using operators.

The hardware description language chosen was VHDL (Very high speed integrated circuit Hardware Description Language).

Hardware description language used in electronic design automation to describe digital and mixed-signal systems such as field-programmable gate arrays and integrated circuits. VHDL can also be used as a general purpose parallel programming language. The IDE on which programs were compiled and simulated was Xilinx’s ISE Design Suite 14.7.

A field-programmable gate array (FPGA) is an integrated circuit designed to be configured by a customer or a designer after manufacturing – hence "field-programmable". The FPGA configuration is generally specified using a hardware description language (HDL), similar to that used for an application-specific integrated circuit (ASIC). (Circuit diagrams were previously used to specify the configuration, as they were for ASICs, but this is increasingly rare.)

FPGAs contain an array of programmable logic blocks, and a hierarchy of reconfigurable interconnects that allow the blocks to be "wired together", like many logic gates that can be inter-wired in different configurations. Logic blocks can be configured to perform complex combinational functions, or merely simple logic gates like AND and XOR. In most FPGAs, logic blocks also include memory elements, which may be simple flip-flops or more complete blocks of memory.

**Reaction Timer**

An electronic device which records a reflex reaction of a human by putting him/her into some situation and delivers the time duration between the event and the reaction. Our module consist of:

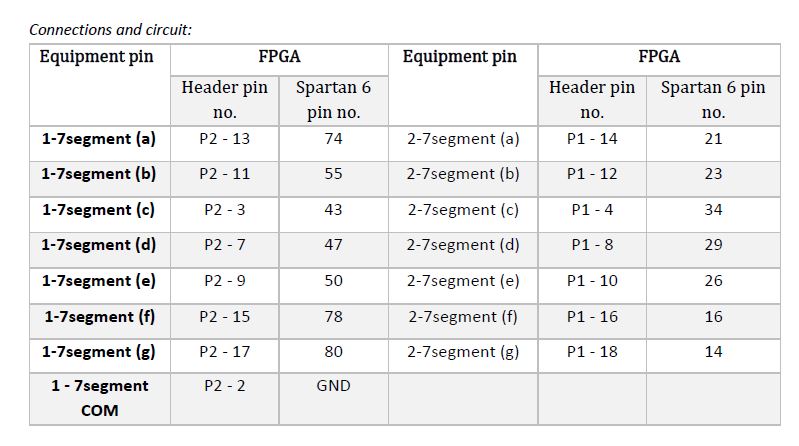
* Event: Button ‘A’ pressed by the User
* Reflex/ Reaction: Button ‘B’ pressed by User

Calculation of time duration would be the difference in pressing of button A and button B

Resetting of timer will also be incorporated, along with LEDs verifying that whether button is pressed or not.

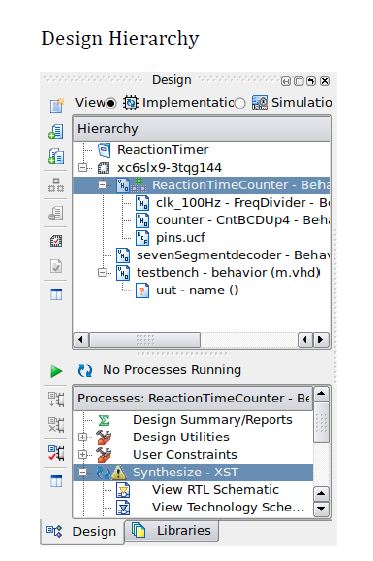
Equipment required:

* FPGA board – 1
* Micro USB cable(for programming and power) – 1
* LEDs (incorporated in FPGA module)
* Push buttons – 3
* 7-segment – 2
* Breadboard – 1
* Jumper wires

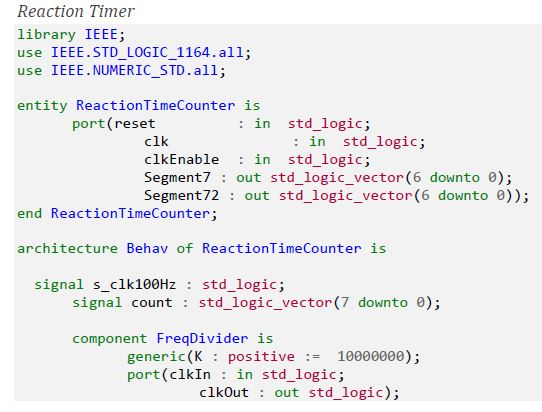


* SW1 -> Switch for Reaction/ Stop -> P126
* SW2 -> Switch for Resetting (Reset) -> P123
* SW3 -> Switch for Starting the event (Start) -> P124
* D8 -> LED for start of event -> P116

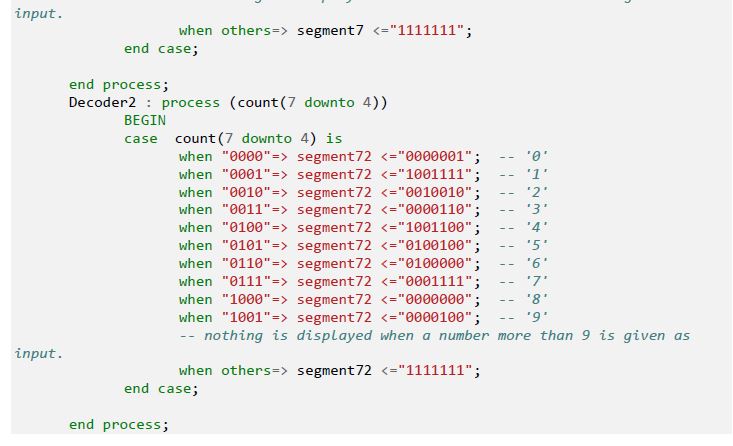
The reaction timer shall begin as soon as “Start” button is pressed, both the 7segments shall start deriving showing the time elapsed and LED will glow, the reaction/ reflex is reflected by pressing the “Stop” button. The LED will stop glowing and both the 7 segments shall stop, and would display the time taken by reaction to happen, thus accomplishing the task. Then one needs to press the Reset button for bringing the timer to zero state.

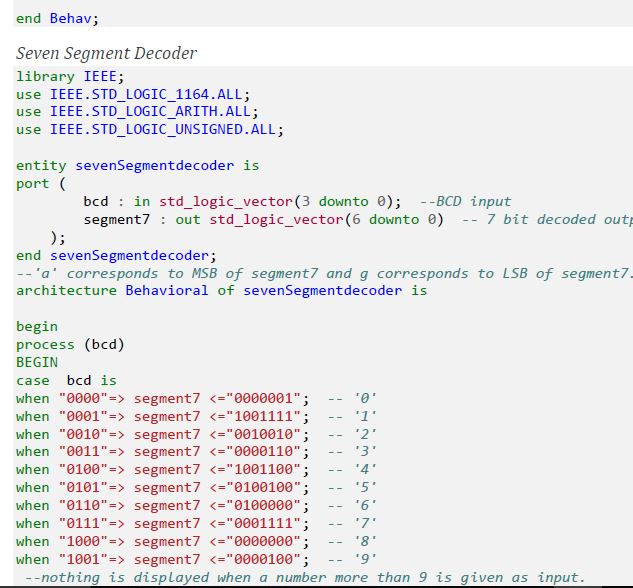


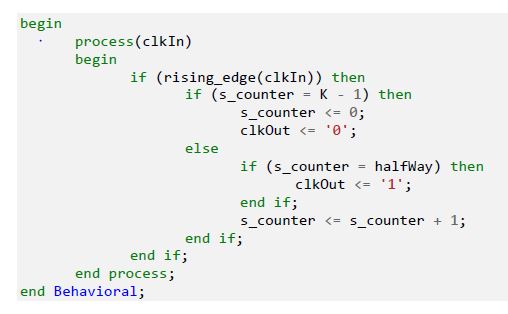
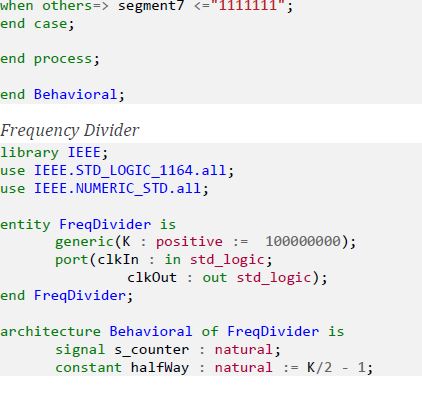
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